UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,120	11/18/2003	Jung-Bae Lee	8021-174 (SS-18151-US)	6097

22150 7590 06/08/2005

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,120	LEE, JUNG-BAE	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7-12,16-18,21 and 24* is/are rejected.

7)☒ Claim(s) *2-6,13-15,19,20,22,23 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 2 is objected to because of the following informalities:

In claim 2, "a mode set register" on lines 5-6 appears to be --a mode register set--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7-9, 10-12, 16-18, 21 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Greeff et al. (US PAT No. 6,356,106).

Regarding claim 1, Fig. 1 of Greeff et al. teaches an on-die termination ("ODT") circuit for use in a synchronous memory device, the ODT circuit comprising; termination voltage port (VTERM) for receiving a termination voltage; a data input/output ("I/O") port (node where 112 and 114 intersect); a first termination resistor (RTERM), one end of which is connected to the data I/O port (RTERM coupled to the node); a switch (122) that selectively connects the other end of the first termination resistor to and the termination voltage port in response to a termination enable signal (TERMINATION ENABLE).

Regarding claim 7, Fig. 1 of Greeff et al. teaches the ODT circuit of claim 1 where the termination voltage is generated by a voltage regulator (Fig. 2; the output voltage of the voltage divider 220 is controlled or regulated by signals ENP and ENN , thus the voltage divider 220 is a voltage regulator; see col. 6, lines 14-39) included in a system to which the synchronous memory device is attached (220 can be used in any/all of the devices 110 of system 100; col. 5, lines 39-41).

Regarding claim 8, Fig. 1 of Greeff et al. teaches the ODT circuit of claim 1 where the termination voltage is generated by a memory controller (110a being a memory controller; col. 5, lines 3-6) included in a system to which synchronous memory device is attached.

Regarding claim 9, Fig. 1 of Greeff et al. teaches the ODT circuit of claim 1 where there is at least one termination voltage port (node for VTERM).

Regarding claim 10, Fig. 1 of Greeff et al. teaches an ODT method for a synchronous memory device, the method comprising: installing a termination voltage port (node for VTERM) in the synchronous memory device, the termination voltage port receiving a termination voltage (VTERM), installing a first termination resistor (122) in the synchronous memory device, the first termination resistor having one end connected to a data I/O port (node where 112 and 114 intersect) in the synchronous

memory device; and selectively connecting the other end of the first termination resistor to the termination voltage port (connection controlled by TERMINATION ENABLE).

Regarding claim 11, Fig. 1 of Greeff et al. teaches an ODT method of claim 10, where selectively connecting the other end of the first termination resistor is performed in a valid section of input data during write operations of the synchronous memory device (110a receiving data, i.e. writing operation; col. 5, lines 1-9).

Regarding claim 12, Fig. 1 of Greeff et al. teaches an ODT method of claim 10, where selectively connecting the other end of the first termination resistor is performed in periods other than read operations of the synchronous memory device (110a receiving data, i.e. writing operation not read operation; col. 5, lines 1-9).

Regarding claim 16, Fig. 1 of Greeff et al. teaches an ODT method of claim 10, further comprising generating the termination voltage using a voltage regulator (Fig. 2; the output voltage of the voltage divider 220 is controlled or regulated by signals ENP and ENN , thus the voltage divider 220 is a voltage regulator; see col. 6, lines 14-39), which is included in a system to which the synchronous memory device is attached , and supplying the termination voltage to the termination voltage port (220 can be used in any/all of the devices 110 of system 100; col. 5, lines 39-41).

Regarding claim 17, Fig. 1 of Greeff et al. teaches an ODT method of claim 10, further comprising generating the termination voltage using a memory controller (110a being a memory controller; col. 5, lines 3-6) which is included in a system to which the synchronous memory device is attached and supplying the termination voltage to the termination voltage port (Fig. 2 provides VTERM; col. 5, lines 37-44).

Regarding claim 18, Figs. 1 & 2 of Greeff et al. teaches a memory system comprising a memory controller (device 110 includes a memory controller; col. 3, lines 38-40); a voltage regulator for generating a termination voltage (Fig. 2; the output voltage of the voltage divider 220 is controlled or regulated by signals ENP and ENN , thus the voltage divider 220 is a voltage regulator; see col. 6, lines 14-39); and a synchronous memory device (110b - 110e) that is connected to the memory controller (110a being a memory controller; col. 5, lines 3-6) and the voltage regulator (220 can be used in any/all of the devices 110 of system 100; col. 5, lines 39-41). and includes an ODT circuit (124, 122), where the ODT circuit comprises: termination voltage port (VTERM) for receiving a termination voltage from the memory controller; a data input/output ("I/O") port (node where 112 and 114 intersect) receiving input data from the memory controller or outputs output data to the memory controller; a first termination resistor (RTERM), one end of which is connected to the data I/O port (RTERM coupled to the node); a switch (122) that selectively connects the other end of the first termination resistor to and the termination voltage port in response to a termination enable signal (TERMINATION ENABLE).

Regarding claim 21, Figs. 1 & 2 of Greeff et al. teaches a memory system comprising a memory controller (device 110 includes a memory controller; col. 3, lines 38-40) for generating a termination voltage; and a synchronous memory device (110b - 110e) that is connected to the memory controller (110a being a memory controller; col. 5, lines 3-6) and includes an ODT circuit (124, 122), where the ODT circuit comprises: termination voltage port (VTERM) for receiving a termination voltage from the memory controller; a data input/output ("I/O") port (node where 112 and 114 intersect) receiving input data from the memory controller or outputs output data to the memory controller; a first termination resistor (RTERM), one end of which is connected to the data I/O port (RTERM coupled to the node); a switch (122) that selectively connects the other end of the first termination resistor to and the termination voltage port in response to a termination enable signal (TERMINATION ENABLE).

Regarding claim 24, Figs. 1 & 2 of Greeff et al. teaches a memory system comprising a memory controller (device 110 includes a memory controller; col. 3, lines 38-40) for generating a termination voltage; and a plurality of synchronous memory devices (110b - 110e) that is connected to the memory controller (110a being a memory controller; col. 5, lines 3-6) via a channel (bus 102) and includes an ODT circuit (124, 122), where the ODT circuit is enabled in only at least one of the plurality of the memory devices that is furthest from the memory controller and is disabled in the other memory devices (col. 5, lines 20-36).

Allowable Subject Matter

Claims 2-6, 13-15, 19-20, 22-23 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Greeff et al. teaches an active termination circuit in a multidrop memory system, one of ordinary skill in the art would not have been motivated to modify the teaching of Greeff et al. to further includes, among other things, the specific of generating the termination enable signal in response to a signal output from a mode register set as required by claims 2-6, 13, 19, 22 and 25, and the specifics of the second termination resistor having one end connected to the data I/O port and the other end connected to the termination voltage port as required by claims 14-15, 20 and 23.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Leung et al. (US PAT No. 5,831,467) discloses a termination circuit with power down mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

June 3, 2005